

TITLE OF THE INVENTION

SOLID-STATE IMAGE SENSING APPARATUS AND METHOD OF
OPERATING THE SAME

5

BACKGROUND OF THE INVENTION

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The present invention relates to a solid-state
image sensing apparatus and a method of operating the
10 same and, more particularly, to a solid-state image
sensing apparatus widely used in an image input
apparatus, such as a video camera and a digital still
camera, and a method of driving the solid-state image
sensing apparatus.

15 Recently, technique for reducing the cell size of a
photoelectric conversion element has been actively
developed for increasing resolution using refining
processing. At the same time, since the level of the
output signal from the photoelectric conversion element
20 decreases as the cell size of the photoelectric
conversion element is reduced, an amplification-type
photoelectric conversion apparatus, capable of
amplifying a photo-charge signal then outputting it, has
been getting attention.

25 As such amplification-type photoelectric conversion
apparatuses, there are metal oxide semiconductor (MOS)

type, an amplified MOS imager (AMI), a charge modulation device (CMD), and a base stored image sensor (BASIS), for instance, but not a conventional charge-coupled device (CCD) type. Among these, in a MOS-type

5 photoelectric conversion apparatus, photo-electrons generated by a photodiode, as a photoelectric conversion element, are collected at the gate of a MOS transistor, and the charge at the gate is amplified using a change in potential at the gate caused by the charge and
10 outputted to an output unit in accordance with a driving signal from an operation circuit. Further, a complementary MOS (CMOS) type photoelectric conversion apparatus, among MOS-type photoelectric conversion apparatuses, can be manufactured in CMOS logic LSI
15 processing, in addition, peripheral circuits can be integrally formed on the same chip easily. Furthermore, the CMOS-type photoelectric conversion apparatus can be operated with a low voltage, which saves electrical energy; therefore, it is anticipated as a useful image
20 sensor for a portable device. Since photodiodes, i.e., photoelectric conversion elements, of the CMOS-type image sensor and their peripheral circuits are made in the CMOS logic LSI processing, the photodiodes and the peripheral circuits are collectively called a CMOS image
25 sensor.

The CMOS image sensor has one or more MOS field effect transistors (FETs) in each cell (pixel). Especially, the CMOS image sensor having a MOS FET for amplification (referred to as "MOS amplifier"

5 hereinafter) whose gate accumulates photo-charge in each pixel can read a carrier signal generated by the photoelectric conversion element in a predetermined period, therefore, is used for a high-sensitive image sensing apparatus.

10 In such a CMOS image sensor, the output signal level is increased by amplifying photo-charge using the MOS amplifier provided in each pixel; however, at the same time, irregularity in threshold voltages V_{th} and gain of the MOS amplifier causes deterioration of the
15 S/N ratio. Especially, it is not possible to restrain irregularity in the threshold voltages V_{th} below several millivolts under the current manufacturing technique. Further, the saturation voltage of the MOS amplifier is in some volts range since the saturation voltage depends
20 upon the voltage of the power supply. Therefore, the S/N ratio is a three-digit number at best, and it is very difficult to achieve 70 to 80dB, which is the demand of the market.

In order to overcome the above problem, a read
25 circuit using a capacitive clamp circuit, as shown in Fig. 17, is disclosed in the Japanese Patent Application

Laid-Open No. 4-61573. Fig. 18 shows an equivalent circuit of a pixel of a solid state image sensing apparatus disclosed in the above reference. Below, the operation of the image sensing apparatus is briefly explained with reference to the equivalent circuit of a pixel shown in Fig. 18 and the timing chart shown in Fig. 19.

Referring to Fig. 18, in advance of reading of photo-charge from a photodiode D1, signals Φ_{CR1} , Φ_{CR2} and Φ_{CS1} at time t_{31p} are changed to high, thereby a MOS switch Q16 is turned on; in turn, a vertical signal line VL3 becomes a ground level, and capacitors C1 and C3 are reset to a voltage VSS. Thereafter, a signal Φ_{CR1} is changed to a low level at time t_{32p} , further, a reset signal Φ_{RS} is changed to a high level, thereby the gate of the MOS amplifier Q2 is reset to a voltage VRS.

Then, at time t_{33p} , the reset signal Φ_{RS} is changed to a low level and a signal Φ_{V3} is changed to high, thereby a MOS FET Q3 for selection (referred to as "MOS selector" hereinafter) is turned on, and an operation voltage VDD is provided to the drain of the MOS amplifier Q2. Accordingly, a voltage VN corresponding to the gate voltage of the MOS amplifier Q2 appears on the vertical signal line VL3 (noise signal).

Next, the signal Φ_{CR2} is changed to low at time t_{34p} , which puts the output side of the capacitor C1 and one

electrode of the capacitor C3 in a floating state. At this time, the signal $\Phi V3$ is changed to low to turn the MOS selector Q3 off. Then, the signal $\Phi CR1$ is changed to high to reset the vertical signal line VL3, thereby
5 the potential of the output side of the capacitor C1 and one electrode of the capacitor C3 becomes a potential, $VSS - VN'$, that is the bias voltage VSS is reduced by a voltage VN' , which is a part of the voltage VN, corresponding to the ratio of the capacitance of the
10 capacitor C1 to the total capacitance of the capacitors C1 and C3. Here, VN' is expressed by the following equation (1).

$$VN' = C1 \times VN / (C1 + C3) \quad \dots (1)$$

15

Next at time t_{3sp} , the signal $\Phi CR1$ is changed to low, the signal $\Phi V3$, applied to the gate of the MOS selector Q3, and a signal ΦVG , applied to the gate of a MOS FET Q1 for transferring photo-charge (referred to as "MOS
20 switch" hereinafter), are changed to high. Accordingly, the MOS switch Q1 is turned on, and the photo-charge generated by the photodiode D1 is transferred to an input capacitor CP. At the same time, the MOS selector Q3 is turned on, and the operation voltage VDD is
25 provided to the drain of the MOS amplifier Q2 via the MOS selector Q3, thereby a voltage VS, corresponding to

the gate voltage of the MOS amplifier Q2 appears on the vertical signal line VL3 (photo-charge signal).

With the aforesaid operation, a voltage across the capacitor C1 is increased by a voltage VS', which is a part of the voltage VS, corresponding to the ratio of the capacitance of the capacitor C1 to the total capacitance of the capacitors C1 and C3, and becomes VSS - VN' + VS'.

Here, the voltage VS' is expressed by the following equation (2), similarly to the voltage VN'.

$$VS' = C1 \times VS / (C1 + C3) \quad \dots (2)$$

Therefore, the final voltage, VC3, across the capacitor C3 is,

$$VC3 = VSS - C1 \times (VN - VS) / (C1 + C3) \quad \dots (3)$$

Thus, a high S/N signal, from which irregularity in the thresholds Vth of a MOS FET for resetting and of a MOS amplifier is reduced, is obtained as seen in the second term, (VN - VS).

In improving the S/N ratio of a CMOS image sensor, while taking measures to reduce fixed pattern noise by providing an image sensing apparatus and method of driving the apparatus as described above, it is also

necessary to increase the maximum allowable charge (Qsat) so as to improve the S/N ratio with regard to random noise which occurs when displaying a moving image.

In a solid-state image sensing apparatus having a photoelectric conversion element, a transfer switch, and a field effect transistor (FET) for amplification whose gate accumulates photo-charge from the photoelectric conversion element of each pixel, a capacitance of a capacitor C which is connected to the gate of the FET (corresponding to the capacitor Cp in the aforesaid example) affects the maximum charge capable of being transferred, namely, the maximum allowable charge Qsat, when transferring photo-charge generated by the photoelectric conversion element to the gate of the FET.

The reason for this is as follows. If the charge to be transferred is electrons, relationship V_g (gate voltage) $> V_{pd}$ (voltage generated by photodiode) should hold for the charge to be transferred. However, since the drop of the gate voltage V_g when unit charge is transferred is inverse-proportional to the capacitance C, if the capacitance C is small, the drop the gate voltage V_g is large in response to a small transferred charge. When the FET is a MOS FET, then the gate capacitance of the MOS FET is also included in the capacitance C. Since the gate capacitance of the MOS FET changes in accordance with its operation state, the maximum

allowable charge Q_{sat} changes depending upon the operation state of the MOS FET when transferring charge.

The aforesaid problem is not considered in the conventional operating method. In the conventional operating method as shown in Fig. 19, for instance, when transferring charge by applying a pulse Φ_{VG} to the gate of the MOS switch Q1, the source of the MOS amplifier Q2 connecting to the vertical signal line VL3 is in a floating state, therefore, the operation of the MOS amplifier Q2 is not determined. If the MOS amplifier Q2 is in an on state, since the MOS selector Q3 is also on when transferring charge, the voltage VDD is applied to the drain of the MOS selector Q3, thus the MOS amplifier Q2 is put into the saturation region and the gate capacitance is reduced comparing to a case of operating in the triode (linear) region. Therefore, problems result from unsteadiness of a floating state when reading photo-charge from the photoelectric conversion element and change in a linear operation range of the MOS amplifier Q2.

Further, in order to increase sensitivity upon transferring photo-charge from the capacitor C3 to a common output line, the capacitor C3 needs to have capacitance of several pF. In addition, in order to increase sensitivity, when reading photo-charge from each pixel, which is determined by a part of the second

term of equation (3), namely $C1/(C1 + C3)$, the capacitor C1 needs to have a capacitance of least several times larger than the capacitance of the capacitor C3. However, due to limitation on the chip size and manufacturing cost, satisfactory sensitivity can not always be obtained.

Furthermore, in the aforesaid method of reading photo-charge, when reading a noise signal, the output side of the capacitor C1 is reset to the voltage VSS, whereas, when reading a photo-charge signal, the output side of the capacitor C1 is in a floating state. In the floating state, for the photodiode D1, the capacitance of the capacitors C1 and C3 connected in parallel becomes the capacitance of the capacitor C1. Therefore, there is no problem if reading operation is performed by taking a sufficiently long time; however, if reading operation is performed in a short time, the initial potential of the vertical signal line when outputting a noise signal and the initial potential of the vertical signal line when outputting a photo-charge signal are different, which makes it difficult to reduce noise at high precision.

In addition, in the aforesaid method of reading signals, the voltage for resetting the vertical signal line VL3 must be sufficient to turn on the MOS amplifier

Q2 for every signal level inputted to the gate of the MOS amplifier Q2, thus restricts the reset voltage.

Besides the aforesaid reference, the concept of resetting the vertical signal line VL3 is disclosed in, e.g., the Japanese Patent Application Laid-Open No. 58-48577 and the Japanese Patent Publication No. 5-18309 for preventing interference between pixels, such as leakage of charge, in a photoelectric conversion element having non-destructive reading characteristics.

Operation of the aforesaid references is briefly explained with reference to the block diagram in Fig. 20 showing a sensor area of a solid-state image sensing apparatus disclosed in the foregoing references, a circuit diagram in Fig. 21 showing a horizontal switch circuit, and a timing chart in Fig. 22.

At time t_{op} , a signal ΦP_{v1} becomes high, and MOS switches S^1_1 to S^{768}_1 which are connected to a vertical signal line V1 of a sensor array C^j_i are turned on, thereby photo-charges in cells (pixels) C^1_1 to C^{768}_1 are outputted to signal output lines B1 to B768.

Slightly after the time t_{op} , at time t_{1p} , a signal ΦP_{H1} applied to the horizontal signal line H1 becomes high. Accordingly, MOS switches Q^1_1 to $Q^{1_{32}}_1$ in a horizontal switch circuit are turned on, thereby photo-charge on the left-most signal output line in each of the 32 sub-groups, each includes 24 signal output lines,

of the signal output lines B1 to B768 is outputted to
multiplexing output lines A1 to A32. Signals on the
multiplexing output lines A1 to A32 are outputted
through amplifiers T1 to T32, respectively. Each of the
5 amplifiers T1 to T32 comprises a pair of differential
transistors both connected between a common constant
current source and ground. To the base of one of the
transistors, an analog pixel (photo-charge) signal is
inputted, whereas to the base of the other transistor, a
10 dark voltage from a pixel which is shielded from light
is inputted. Then an analog signal obtained by
subtracting the dark voltage from the analog pixel
signal is outputted.

Then, the signal $\Phi_{P_{H1}}$ applied to the horizontal
15 signal line H1 becomes low, and a signal $\Phi_{P_{H2}}$ on a
horizontal signal line H2 becomes high at time t_{2p} .
Accordingly, the MOS switches Q^2_1 to Q^2_{32} in a horizontal
switch circuit are turned on, thereby pixel signals on
signal output lines which are the second to the left-
20 most lines in the respective 32 sub-groups of signal
output lines B1 to B768 are outputted to multiplexing
output lines A1 to A32. Similarly, signals to be applied
to the horizontal signal lines H3 to H24 sequentially
become high, and analog pixel signals of the respective
25 sub-groups are outputted. After the signal $\Phi_{P_{H24}}$ applied
to the last horizontal signal line H24 becomes low, the

signal $\Phi_{P_{V1}}$ applied to the vertical signal line V1 becomes low, thereby scanning of all the cells connected to the signal line V1 is completed.

Thereafter, before start of reading the cells
5 connected to the signal line V3, a blanking period elapses. During the blanking period, signals $\Phi_{P_{H1}}$ to $\Phi_{P_{H24}}$ applied to the horizontal signal lines H1 to H24 are turned to high, thereby connecting all the signal output lines B1 to B768 to the corresponding output
10 lines A1 to A32. At the same time, a signal Φ_{P_R} on a refresh line R is turned to high and MOS switches R1 to R32 are turned on, thereby the multiplexing output lines A1 to A32 are grounded. Accordingly, all the signal output lines B1 to B768 are grounded, and residues of
15 pixel signals remaining from the previous scanning are cleared.

However, there are the following problems in the aforesaid configuration, which will be explained below with reference to Fig. 23. Fig. 23 shows a case of
20 reading pixel signals from the cells connected to the vertical signal line V1. In Fig. 23, a signal voltage of the cell C_1^1 is denoted by VS1, similarly, signal voltages of the cells C_1^2 to C_1^{24} are denoted by VS2 to VS24, respectively. Further, parasitic capacitance of
25 the signal output lines B1 to B24 is denoted by C11, parasitic capacitance connected to the base of the

transistor connected to the differential transistor T1 is denoted by C21, the common signal output line is A1, and a signal voltage inputted to the base of the transistor is denoted by VSO. Then, a signal voltage VSO' when a signal on the signal output line B1 is read out is expressed by the following equation (4).

$$VSO' = (C21 \times VSO + C11 \times VS1) / (C21 + C11) \dots (4)$$

Further, a signal voltage VSO" when a signal on the signal output line B2 is read out is expressed by the following equation (5).

$$VSO'' = (C21 \times VSO' + C11 \times VS2) / (C21 + C11) \dots (5)$$

15

In order to prevent interference between adjoining pixels by resetting the gate of the MOS switch R1 by applying the reset pulse Φ_{P_r} only during the blanking period, it is necessary to reduce $C21 \times VSO'$ in equation (5) by making the capacitance of the capacitor C11 much larger than the capacitance of the capacitor C21. However, when the capacitance of the capacitor C11 is increased, the capacitance upon transferring a signal from a cell also increases, thereby sensitivity decreases.

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SUMMARY OF THE INVENTION

The present invention has been made in consideration of the above situation, and has as its
5 object to improve the S/N ratio and widen the dynamic range of image signals obtained from a solid-state image sensing apparatus.

According to the present invention, the foregoing object is attained by providing a method of operating a
10 solid-state image sensing apparatus having pixels each including a photoelectric conversion element, a field effect transistor whose gate receives photo-charge generated by the photoelectric conversion element, and a transfer switch for controlling connection between the
15 photoelectric conversion element and the gate of the field effect transistor, wherein transference of the photo-charge from the photoelectric conversion element to the gate of the field effect transistor is performed under a condition that a channel is formed under the
20 gate of the field effect transistor.

Further, the foregoing object is also attained by providing a method of operating a solid-state image sensing apparatus having pixels each including a photoelectric conversion element, a field effect
25 transistor whose gate receives photo-charge generated by the photoelectric conversion element, a first switch for

controlling connection between the photoelectric
conversion element and the gate of the field effect
transistor, and a first reset means for resetting the
gate of the field effect transistor, and output lines
5 for transferring an output from the field effect
transistors, load means, provided on the output lines,
for the field effect transistors, and second reset means
for resetting the output lines to a predetermined
voltage, wherein the output lines are reset by the
10 second reset means in advance of connecting of the
photoelectric conversion element and the gate of the
field effect transistor.

Further, the foregoing object is also attained by
providing a solid-state image sensing apparatus having
15 pixels each including a photoelectric conversion element,
a field effect transistor whose gate receives photo-
charge generated by the photoelectric conversion element,
and a transfer switch for controlling connection between
the photoelectric conversion element and the gate of the
20 field effect transistor, comprising control means for
controlling that transference of the photo-charge from
the photoelectric conversion element to the gate of the
field effect transistor is performed under a condition
that a channel is formed under the gate of the field
25 effect transistor.

Further, the foregoing object is also attained by providing a solid-state image sensing apparatus having pixels each including a photoelectric conversion element, a field effect transistor whose gate receives photo-charge generated by the photoelectric conversion element, a first switch for controlling connection between the photoelectric conversion element and the gate of the field effect transistor, and a first reset means for resetting the gate of the field effect transistor, and output lines for transferring an output from the field effect transistors, comprising load means, provided on the output lines, for the field effect transistors; and second reset means for resetting the output lines to a predetermined voltage.

Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and, together

with the description, serve to explain the principles of the invention.

Fig. 1 is a timing chart showing operation timing according to a first embodiment of the present invention;

Fig. 2 is a timing chart showing operation timing according to a second embodiment of the present invention;

Fig. 3 is a circuit diagram of a part of a solid-state image sensing apparatus according to the second embodiment of the present invention;

Fig. 4 is a timing chart showing operation timing according to a third embodiment of the present invention;

Fig. 5 is a circuit diagram of a part of a solid-state image sensing apparatus according to the third embodiment of the present invention;

Fig. 6 is a timing chart showing operation timing according to a fourth embodiment of the present invention;

Fig. 7 is a circuit diagram of a part of a solid-state image sensing apparatus according to the fourth embodiment of the present invention;

Fig. 8 is a timing chart showing operation timing according to a fifth embodiment of the present invention;

Fig. 9 is a circuit diagram of a part of a solid-state image sensing apparatus according to the fifth embodiment of the present invention;

Fig. 10 is a timing chart showing operation timing according to a sixth embodiment of the present invention;

Fig. 11 is a circuit diagram of a part of a solid-state image sensing apparatus according to the sixth embodiment of the present invention;

Fig. 12 is a conceptual view of a configuration of a vertical scan circuit of the solid-state image sensing apparatus shown in Fig. 11;

Fig. 13 is a block diagram illustrating a configuration of a solid-state image sensing apparatus according to a seventh embodiment of the present invention;

Fig. 14 is a circuit diagram illustrating a main configuration of a pixel;

Fig. 15 is a timing chart showing operation timing according to the seventh embodiment of the present invention;

Fig. 16 is a circuit diagram illustrating a main portion of a pixel according to an eighth embodiment of the present invention;

Fig. 17 is a circuit diagram of a conventional solid-state image sensing apparatus;

Fig. 18 is a circuit diagram corresponding to a single pixel of the conventional solid-state image sensing apparatus shown in Fig. 17;

Fig. 19 is a timing chart for explaining an operation of the conventional solid-state image sensing apparatus;

Fig. 20 is a diagram of a sensor area of another conventional solid-state image sensing apparatus;

Fig. 21 is a circuit diagram of a horizontal switch circuit of the conventional solid-state image sensing apparatus;

Fig. 22 is a timing chart for explaining an operation of the conventional solid-state image sensing apparatus; and

Fig. 23 is an explanatory view for explaining a problem of the conventional solid-state image sensing apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described in detail below in accordance with the accompanying drawings.

<First Embodiment>

As the first embodiment, a case where the solid-state image sensing apparatus as shown in Fig. 18 is

driven at timing as shown in a timing chart in Fig. 1 is explained. The solid-state image sensing apparatus provides photo-charge, generated by the photodiode D1 in accordance with the quantity of light, to the MOS
5 amplifier Q2 via the MOS switch Q1, then turns on the MOS selector Q3 to transfer the photo-charge to a vertical signal line VL3.

In advance of reading of the photo-charge from a photodiode D1, the signals Φ_{CR1} , Φ_{CR2} and Φ_{CS1} at time
10 t_1 are changed to high, thereby a MOS switch Q16 is turned on; in turn, the vertical signal line VL3 becomes a ground level, and the capacitors C1 and C3 are reset to the voltage VSS. Thereafter, the signal Φ_{CR1} is changed to a low level at time t_2 , further, the reset
15 signal Φ_{RS} is changed to a high level, thereby the gate of the MOS amplifier Q2 is reset to the voltage VRS.

Then, at time t_3 , the reset signal Φ_{RS} is changed to a low level and the signal Φ_{V3} is changed to high, thereby the MOS selector Q3 is turned on, and the
20 operation voltage VDD is provided to the drain of the MOS amplifier Q2. Accordingly, a voltage VN corresponding to the gate voltage of the MOS amplifier Q2 appears on the vertical signal line VL3 (noise signal).

25 Next, the signal Φ_{CR2} is changed to low at time t_4 , which puts the output side of the capacitor C1 and one

electrode of the capacitor C3 in a floating state. At this time, the signal $\Phi V3$ is changed to low to turn the MOS selector Q3 off. Then, the signal $\Phi CR1$ is changed to high to reset the vertical signal line VL3, thereby
5 the potential of the output side of the capacitor C1 and one electrode of the capacitor C3 becomes a potential, $VSS - VN'$, that is, the bias voltage VSS is reduced by a voltage VN' , which is a part of the voltage VN, corresponding to the ratio of the capacitance of the
10 capacitor C1 to the total capacitance of the capacitors C1 and C3.

Next at time t_5 , the signal ΦVG applied to the gate of the MOS switch Q1 is changed to high, and photo-charge is transferred from the photodiode D1 to the gate
15 of the MOS amplifier Q2. At this time, the signal $\Phi CR1$ is kept high to fix the source of the MOS amplifier Q2 to a ground level, and the signal $\Phi V3$ is set to low to cut the supply of the voltage VDD to the drain of the MOS amplifier Q2, thereby it is possible to restrain the
20 operational range of the MOS amplifier Q2 to the triode region. More specifically, during a period between time t_4 , when the signal $\Phi V3$ is set to low, and the time t_5 , when the signal ΦVG is set to high, a potential at the drain of the MOS amplifier Q2 decreases to near the
25 ground level, thereby a bias relationship between the gate and the drain of the MOS amplifier Q2, namely a

potential difference between the gate and the drain of the MOS amplifier Q2 is greater than a threshold, is maintained.

To the gate of the MOS amplifier Q2 whose operational range is limited to the triode region, a capacitance of oxide film, having a large area determined by the gate width and the gate length, is added. Accordingly, the maximum allowable charge increases.

Thereafter, the signal Φ_{VG} is changed to low at time t_6 , then, the signal Φ_{CR1} is changed to low and the signal Φ_{V3} is changed to high at time t_7 , a voltage V_S corresponding to the photo-charge transferred to the gate of the MOS amplifier Q2 appears on the vertical signal line VL3 (photo-charge signal). Accordingly, the potential at the output side of the capacitor C1 and one electrode of the capacitor C3 becomes $(V_{SS} - V_{N'} + V_{S'})$.

Comparing to the operation method as described with reference to Fig. 19, charge which can be dealt with in the linear operation region (i.e., maximum allowable charge) is increased since the gate capacitance of the MOS amplifier, while transferring the charge, is increased, and the maximum allowable charge is increased by 15%, although there is no difference in the noise removal rate of fixed pattern noise between the

conventional method and the method of the present invention.

In the operation method according to the first embodiment, transference of a photo-charge signal from a photodiode of a photoelectric conversion element to the gate of a field effect transistor (FET) which functions as an amplifier is performed under a condition that the channel is formed under the gate of the FET by the reset voltage VRS, and the gate voltage is lowered by the transferred charge. Accordingly, a voltage corresponding to the lowered gate voltage appears on a vertical signal line.

In other words, while transferring the photo-charge signal from a photodiode of a photoelectric conversion element to the gate of a field effect transistor which functions as an amplifier, the gate voltage of the FET is higher than the sum of the source voltage and the threshold voltage of the FET.

<Second Embodiment>

Next, an example of operating a solid-state image sensing apparatus as shown in Fig. 3 in accordance with timing shown in Fig. 2 is explained in the second embodiment.

First, a circuit configuration of the solid-state image sensing apparatus as shown in Fig. 3 is explained.

Each pixel includes a photodiode 1, a transfer switch 2, a reset switch 3, a pixel amplifier 4, and a row selection switch 5 and a plurality of such pixels are connected as shown in Fig. 3. Note, only four pixels are shown in Fig. 3, however, a number of pixels are arranged in practice. When the row selection switch 5 is turned on, a source follower, configured with a source of load current 7 and the pixel amplifier 4, starts operating, and signals of a selected row are transferred to respective vertical output lines 6. The signals are stored in signal storage unit 11 via respective transfer gates 8. The signals, temporarily stored in the signal storage unit 11, are sequentially transferred to an output unit (not shown) via a horizontal scan circuit 12.

Next, the case of operating the solid-state image sensing apparatus as shown in Fig. 3 in accordance with operation timing shown in Fig. 2 is explained below. First, a signal Φ_{RES} becomes high at t_{21} , then the gate of the pixel amplifier 4 is reset to a reset potential (potential of pulse Φ_{RES} minus threshold potential). Thereafter, a signal Φ_{SEL} becomes high at time t_{22} , and the source follower, configured with the pixel amplifier 4 and the source of load current 7, starts operating. Accordingly, noise corresponding to the reset potential appears on the corresponding vertical output line 6, and is temporarily stored in the signal storage unit 11 by

changing a signal Φ_{TN} to high as well as turning a transfer gate 13 on. After reading the noise signal, the signals Φ_{SEL} and Φ_{TN} are changed to low at time t_{23} , and the potential of the vertical output line 6 decreases as load current is supplied from the source of current 7. When the potential of the vertical output line 6 decreases to near ground voltage, a transfer signal Φ_{TX} becomes high at time t_{24} , and photo-charge is transferred from each photodiode 1 to the gate of the pixel amplifier 4.

At this time, no voltage is provided to the drain of the pixel amplifier 4, thus, the pixel amplifier 4 operates in the triode region. Therefore, the gate capacitance of the pixel amplifier becomes the maximum. Thereafter, the signal Φ_{TX} is changed to low at time t_{25} , then the signals Φ_{SEL} and Φ_{TS} are changed to high at time t_{26} , and the photo-charge are read out.

By controlling a period between the time t_{25} when the signal Φ_{TX} is changed to low, and the time t_{26} when the signals Φ_{SEL} and Φ_{TS} are changed to high, it is possible to operate the pixel amplifier 4 in a linear operation region, thereby a photo-charge signal is obtained in a wide dynamic range.

When photo-charge is transferred from the photodiode 1 to the pixel amplifier 4 according to the second embodiment, since the operation of the pixel

amplifier 4 is limited to the triode region, the maximum allowable charge is increased by 11% comparing to the conventional operation method.

5 <Third Embodiment>

Next, an example of operating a solid-state image sensing apparatus as shown in Fig. 5 in accordance with timing shown in Fig. 4 is explained in the third embodiment.

10 First, a circuit configuration of the solid-state image sensing apparatus as shown in Fig. 5 is explained. Each pixel includes a photodiode 1, a transfer switch 2, a reset switch 3, a pixel amplifier 4, and a row selection switch 5 and a plurality of such pixels are
15 connected as shown in Fig. 5. Note, only four pixels are shown in Fig. 5, however, a number of pixels are arranged in practice. When the row selection switch 5 is turned on, a source follower, configured with a source of load current 7 and the pixel amplifier 4, starts
20 operating, and signals of a selected row are transferred to respective vertical output lines 6. The signals are stored in signal storage unit 11 via respective transfer gates 8. The signals, temporarily stored in the signal storage unit 11, are sequentially transferred to an
25 output unit (not shown) via a horizontal scan circuit 12. Further, vertical-output-line reset switches 9 for

resetting the vertical output lines 6 to a fixed potential are also provided. Differences between Fig. 5 and Fig. 3 are that the vertical-output-line reset switches 9 are provided and a reset pulse Φ_{VR} is supplied to the gate of the reset switches 9 in Fig. 5.

Next, a case of operating the solid-state image sensing apparatus as shown in Fig. 5 in accordance with operation timing shown in Fig. 4 is explained below. First, the signal Φ_{VR} becomes high at t_{31} , and the vertical output lines 6 are reset to a fixed potential (ground potential in the third embodiment). After the signal Φ_{VR} is changed to low at time t_{32} , a signal Φ_{RES} becomes high at t_{33} , then the gate of the pixel amplifier 4 is reset to a reset potential. Thereafter, the signal Φ_{RES} is changed to low, and signals Φ_{SEL} and Φ_{TN} become high at time t_{34} . Accordingly, the source follower, configured with the pixel amplifier 4 and the source of load current 7, starts operating, and noise corresponding to the reset potential appears on the corresponding vertical output line 6, and is temporarily stored in the signal storage unit 11 by turning on the transfer gate 13.

After reading the noise signal at time t_{35} , the signal Φ_{VR} becomes high at time t_{36} , and the vertical output lines 6 are again reset to the ground potential. During a period when the vertical output lines 6 are

reset, the transfer signal Φ_{TX} becomes high at time t_{37} ,
in turn, photo-charge is transferred from the photodiode
1 to the gate of the pixel amplifier 4. At this time,
the source of the pixel amplifier (MOS FET) 4 is fixed
5 to the ground potential to which the vertical output
lines 6 are reset. Further, since the drain of the pixel
amplifier 4 is not supplied with a voltage, the
operation of the pixel amplifier 4 is limited to the
triode region.

10 After photo-charge is transferred to the gate of
the pixel amplifier 4 at time t_{38} , the signals Φ_{SEL} and
 Φ_{TS} are changed to high at time t_{39} , and the photo-charge
is transferred to the corresponding vertical output line
6, further, read out to the signal storage unit 11 by
15 turning on the transfer gate 8. In the second embodiment,
it is necessary to supply sufficiently large current
from the source of current 7 for decreasing the
potential at the source of the pixel amplifier 4 to near
the ground potential when transferring charge, or to
20 lengthen a blank period after noise is read out until
photo-charge is transferred. In the third embodiment, in
contrast, the vertical output lines 6 can be reset,
therefore, there is no such limitation as described
above associated with the configuration of the
25 photoelectric conversion element as described in the
second embodiment.

Further, if the potential of the vertical output line 6 changes while the gate potential of the pixel amplifier 4 is in the floating state, a feed-back phenomenon is caused by gate-source capacitance of the pixel amplifier 4. In the third embodiment, the potential of the vertical output line 6 always increases from the ground potential, the ratio of the feed-back voltage to the voltage of the photo-charge is kept constant, and the photo-charge output is kept linear as an additional effect.

Comparing to the conventional operation method, the maximum allowable charge Q_{sat} is increased by 13% according to the third embodiment, since the gate capacitance of the pixel amplifier 4 is maximum when transferring photo-charge to the gate of the pixel amplifier 4.

<Fourth Embodiment>

Next, an example of operating a solid-state image sensing apparatus as shown in Fig. 7 in accordance with timing shown in Fig. 6 is explained in the fourth embodiment.

First, the circuit configuration of the solid-state image sensing apparatus as shown in Fig. 7 is explained. Each pixel includes a photodiode 1, a transfer switch 2, a reset switch 3, a pixel amplifier 4, and a row

selection switch 5 and a plurality of such pixels are connected as shown in Fig. 7. Note, only four pixels are shown in Fig. 7, however, a number of pixels are arranged in practice. The pixel amplifier 4 is connected to a corresponding vertical output line 6 via the row selection switch 5, and when the pixel amplifier 4 and the row selection switch 5 are turned on the pixel amplifier 4, with a resistor 47, operates as an inverse amplifier. Further, vertical-output-line reset switches 9 for resetting the vertical output lines 6 to a fixed potential (ground potential in the fourth embodiment) are also provided. The pixel amplifier 4 in Fig. 7 differs from the pixel amplifier 4 in Fig. 5 in that it operates as an inverse amplifier with the resistor 47.

Next, a case of operating the solid-state image sensing apparatus as shown in Fig. 7 in accordance with operation timing shown in Fig. 6 is explained below. First, a signal Φ_{RES} becomes high at t_{41} , then the gate of the pixel amplifier 4 is reset to a reset potential. Thereafter, signals Φ_{SEL} and Φ_{TN} become high at time t_{42} , the transfer gate 13 is turned on, and noise is read out. After reading the noise signal at time t_{43} , while keeping the signal Φ_{SEL} high, a signal Φ_{VR} is changed to high at time t_{44} , and the vertical output line 6 and the drain of the pixel amplifier 4 are reset to the ground potential. Then, the signals Φ_{SEL} and Φ_{VR} are changed to low at

time t_{45} , accordingly, the drain of the pixel amplifier 4 is put into the floating state while maintaining the ground potential. At this time, the source of the pixel amplifier 4 is grounded, thus, the operation of the pixel amplifier 4 is limited to the triode region.

Under the foregoing state, a signal Φ_{TX} becomes high at time t_{46} , and photo-charge is transferred from the photodiode 1 to the gate of the pixel amplifier 4. Subsequently, the signal Φ_{TX} is changed to low at time t_{47} , the row selection signal Φ_{SEL} and the signal Φ_{TS} are changed to high at time t_{48} . Accordingly, the transfer gates 8 are turned on and the photo-charge signals are read out. Thereafter, the noise signals and the photo-charge signals stored in a signal storage unit 11 are sequentially outputted via a horizontal scan circuit 12 in accordance with a horizontal scan signal $\Phi_H(1, 2)$.

In the fourth embodiment, the pixel amplifier 4 is in the triode state while transferring photo-charge to the gate of the pixel amplifier 4, and the maximum allowable charge Q_{sat} is increased by 25% comparing to the conventional operation method.

<Fifth Embodiment>

Next, an example of operating a solid-state image sensing apparatus as shown in Fig. 9 in accordance with

timing shown in Fig. 8 is explained in the fifth embodiment.

First, a circuit configuration of the solid-state image sensing apparatus as shown in Fig. 9 is explained.

5 Each pixel includes a photodiode 1, a transfer switch 2, a reset switch 3, a pixel amplifier 4, and a row selection switch 5 and a plurality of such pixels are connected as shown in Fig. 9. Note, only four pixels are shown in Fig. 5, however, a number of pixels are

10 arranged in practice. When the row selection switch 5 is turned on, a source follower, configured with a source of load current 7 and the pixel amplifier 4, starts operating, and signals of a selected row are transferred to respective vertical output lines 6. The signals are

15 stored in signal storage unit 11 via respective transfer gates 8. The signals, temporarily stored in the signal storage unit 11, are sequentially transferred to an output unit (not shown) via a horizontal scan circuit 12. Further, vertical-output-line reset switches 9 for

20 resetting the vertical output lines 6 to a fixed potential are also provided. Differences between Fig. 9 and Fig. 5 are that the row selection switch 5 is connected in the side of the source of the pixel amplifier 4, and a noise signal and a photo-charge

25 signal are both read out to the corresponding vertical output line 6 via the row selection switch 5.

and Φ_{TS} are changed to low to finish reading operation of one row, and the process proceeds to operation of reading the next row.

In the fifth embodiment as described above, since
5 the pixel amplifier 4 is always in the on-state while transferring photo-charge from the photodiode 1 to the gate of the pixel amplifier 4, the maximum allowable charge Q_{sat} is increased by 43% comparing to the conventional operation method.

10 Note that, in the fifth embodiment, the solid-state image sensing apparatus has a vertical-output-line reset switches 9, however, they may be omitted if the sources of load current 7 supply sufficiently large current and the source of the pixel amplifiers 4 are quickly
15 decreased to the ground potential before transferring photo-charges to the gate of the pixel amplifiers 4.

<Sixth Embodiment>

Next, an example of operating a solid-state image
20 sensing apparatus as shown in Fig. 11 in accordance with timing shown in Fig. 10 is explained in the sixth embodiment.

First, a circuit configuration of the solid-state image sensing apparatus as shown in Fig. 11 is explained.
25 Each pixel includes a photodiode 1, a transfer switch 2, a reset switch 3, a pixel amplifier 4, and a row

selection switch 5 and a plurality of such pixels are connected as shown in Fig. 11, similarly to Fig. 9. Note, only four pixels are shown in Fig. 11, however, a number of pixels are arranged in practice. When the row selection switch 5 is turned on, a source follower, configured with a source of load current 7 and the pixel amplifier 4, starts operating, and signals of a selected row are transferred to respective vertical output line 6. The signals are stored in signal storage unit 11 via respective transfer gates 8, 14, 15, or 16. The signals, temporarily stored in the signal storage unit 11, are sequentially transferred to an output unit via a horizontal scan circuit 12. Further, vertical-output-line reset switches 9 for resetting the vertical output lines 6 to a fixed potential are also provided. In this solid-state image sensing apparatus, signals in the even-number rows and signals in the odd-number rows are separately transferred to the signal storage unit 11 using the transfer gates 8, 14, 15 and 16. Accordingly, it is possible to read out signals of two rows during horizontal blanking period.

Fig. 12 is a view showing a configuration of a part of a vertical scan circuit 10 of the solid-state image sensing apparatus shown in Fig. 11. With a signal ΦSEL1 for selecting the odd-number rows and a signal ΦSEL2 for selecting the even-number rows which are independently

provided, signals of two rows are transferred to the
signal storage unit 11 in the single horizontal blanking
period. More specifically, the vertical scan circuit 10
includes a vertical shift register 17 which outputs a
5 pulse signal $V(n)$ for selecting a n -th pair of adjoining
odd- and even-number rows, and plural sets of NOR gates
18 to 21, each pair corresponds to each even-and-odd-
number-row pair. A pulse signal $\Phi V(n)$ from the vertical
shift register 17, configured within the vertical scan
10 circuit 10, is inputted to one terminal of each of the
NOR gates 18 to 21 of the n -th set, and the row
selection signals $\Phi SEL1$ and $\Phi SEL2$, a reset signal ΦRES ,
and a transfer signal ΦTX , all of which are generated in
the vertical scan circuit 10, are provided to the other
15 terminals of the NOR gates 18 to 21, respectively. When
the pulse signal $V(n)$, selecting the n -th pair of rows,
is inputted, then the NOR gates 18 to 21 outputs
selection signals $\Phi SEL1(n)$ and $\Phi SEL2(n)$ to the
corresponding rows, and a reset signal $\Phi RES(n)$ and a
20 transfer signal $\Phi TX(n)$ to both of the even and rows of
the n -th pair for operating the respective pixels.

Next, the case of operating the solid-state image
sensing apparatus as shown in Fig. 11 in accordance with
operation timing shown in Fig. 10 is explained below.
25 Note, except the signals $\Phi RES1$ and $\Phi RES2$, $\Phi TS1$ and $\Phi TS2$,
and $\Phi TN1$ and $\Phi TN2$, which are respectively applied for an

odd row and an even row, all the other signals are simultaneously applied to both even- and odd-number rows. Considering an odd-number row, first, a signal Φ_{RES} becomes high at t_{60} , then the gate of the pixel amplifier 4 is reset to a reset potential (potential of pulse Φ_{RES} minus threshold potential). Thereafter, the signals Φ_{SEL1} and Φ_{TN1} becomes high at time t_{61} , and noise in the odd-number row is read out to the signal storage unit 11. After reading the noise signals of the odd-number row, the signals Φ_{SEL1} and Φ_{TN1} are changed to low at time t_{62} , and the signals Φ_{SEL2} and Φ_{TN2} are changed to high at time t_{63} , and noise in the even-number row is read out to the signal storage unit 11 by the time t_{64} .

After reading the noise signals of the even-number row, the signals Φ_{SEL1} , Φ_{SEL2} , and Φ_{VR} become high at time t_{65} , thereby the vertical output line 6 is reset. Note, in the sixth embodiment, the reset potential is the ground potential. Under this state, a signal Φ_{TX} is changed to high, and photo-charge is transferred from the photodiode 1 to the gate of the pixel amplifier 4. As the photo-charge is transferred, the gate potential of the pixel amplifier 4 decreases, however, since the signals Φ_{SEL1} and Φ_{SEL2} are high and the row selection switch 5 is on, the source of the pixel amplifier 4 is fixed to the ground voltage through the row selection switch 5 and the pixel amplifier 4 is always in the on-

state during transferring the photo-charge. Photo-
charges in an odd-number row and an even-number row are
read out to the signal storage units 11 by sequentially
changing the signals ΦSEL1 and ΦTS1 , and ΦSEL2 and ΦTS2
5 to high (at times t_{67} , t_{68} , t_{69} , t_{70}).

By repeating the aforesaid operation, photo-charge
signals are sequentially read out for a frame image.

As a modification of the sixth embodiment, by
adding the photo-charge signals of consecutive even- and
10 odd-number rows, it is possible to obtain signals
conforming to a moving image.

In the conventional operation method, since the
source of the pixel amplifier 4 is in the floating state
while transferring photo-charge to the gate of the pixel
15 amplifier 4, the pixel amplifier 4 is turned off when
large photo-charge is transferred. In contrast, the
pixel amplifier 4 is fixed to the on-state in the sixth
embodiment, the maximum allowable charge Q_{sat} is
increased by 45% comparing to the conventional operation
20 method.

According to the first to sixth embodiments as
described above, photo-charge is transferred to the gate
of a MOS transistor, used as the pixel amplifier 4, in
the optimum operation region of the MOS transistor by
25 supplying operation pulses in various ways, the MOS
transistor operates in the triode region where the MOS

transistor operates linearly, thereby it is possible to read out the photo-charge while widening a dynamic range of the pixel amplifier 4.

Therefore, in the operation methods for operating
5 solid-state image sensing apparatuses as described above, it is possible to increase the maximum allowable charge Q_{sat} .

The foregoing embodiments can be generally applied to any type of solid-state image sensing apparatus
10 having a photoelectric conversion element, a field effect transistor whose gate receives photo-charge, and a transfer switch for controlling the connection between the photoelectric conversion element and the gate of the field effect transistor in each pixel unit, and the
15 maximum allowable charge Q_{sat} which can be dealt with by a source-follower type amplifier and the field effect transistor for inverse amplification is increased, thereby the dynamic range is widened. Accordingly, high-quality image signals of high S/N ratio can be obtained.

20

<Seventh Embodiment>

Fig. 13 is a block diagram illustrating a configuration of a solid-state image sensing apparatus according to the seventh embodiment, and Fig. 14 is a
25 circuit diagram illustrating a basic configuration of a pixel. A plurality of such pixels are formed on a single

semiconductor substrate made of, e.g., mono-crystalline
silicone, in CMOS LSI processing in accordance with a
manufacturing technique of a semi-conductor integrated
circuit, and collectively called as "CMOS sensor" in
5 general. Further, in the seventh embodiment, pixels S11
to S_m_n of the solid-state image sensing apparatus,
arranged in m rows and n columns are explained, and
there is no limitation on the numbers of rows and
columns.

10 First, the basic configuration of each of the
pixels S11 to S_m_n is explained with reference to Fig. 14.
The anode of a photodiode PD which generates photo-
charge is grounded in the seventh embodiment. The
cathode of the photodiode PD is connected to the gate of
15 a MOS transistor M3 for amplification (referred to as
"MOS amplifier" hereinafter) via a charge transfer
switch TX. Further, to the gate of the MOS amplifier M3,
the source of a MOS transistor M1 (referred to as "reset
MOS" hereinafter) for resetting the MOS amplifier M3 is
20 connected. To the drain of the reset MOS M1, a reset
voltage VR is provided. Further, the drain of the MOS
amplifier M3 is connected to a MOS transistor M2
(referred to as "MOS selector" hereinafter) to select a
row to which an operation voltage VDD is applied.

25 Next, referring to Fig. 13, the configuration of
the solid-state image sensing apparatus according to the

seventh embodiment will be explained. The gates of charge transfer switches TX of the pixels S11 to S_mn are connected to first row selection lines (vertical scan lines) TX1 to TX_m each extending in the horizontal direction. For instance, the gates of charge transfer switches TX of pixels S11 to S1_n in the first row are connected to the first row selection line TX1, and similarly, the gates of charge transfer switches TX of pixels Si1 to Si_n (i is an arbitrary integer) in the i-th row are connected to the first row selection line TX_i. Further, the gates of the MOS transistors M1 of the pixels S11 to S1_n are connected to a second row selection line (vertical scan line) RES1 which also extends in the horizontal direction. Similarly, the gates of MOS transistors M1 of pixels Si1 to Si_n in the i-th row are connected to the second row selection line RES_i.

Further, the gates of the MOS transistors M3 of the pixels S11 to S1_n are connected to a third row selection line (vertical scan line) SEL1 which also extends in the horizontal direction. Similarly, the gates of MOS transistors M3 of pixels Si1 to Si_n in the i-th row are connected to the third row selection line SEL_i. These first to third row selection lines TX_i, RES_i, and SEL_i are connected to a vertical scan circuit 71, and applied with voltage signals in accordance with the following

operation timing shown in Fig. 15. To the first to third row selection lines, signals $\Phi TX1$ to ΦTXm , $\Phi RES1$ to $\Phi RESm$, and $\Phi SEL1$ to $\Phi SELm$ are provided from the vertical scan circuit 71.

5 The sources of the MOS transistors M3 of the pixels S11 to S_{m1} are connected to a vertical signal line V1 which extends in the vertical direction. Similarly, the sources of the MOS transistors M3 of pixels S1j to S_{mj} (j is an arbitrary integer) in the j-th column are
10 connected to a vertical signal line Vj. Further, taking the vertical signal line V1 as an example, it is connected to a constant current source I1 which is a load, as well as applied with a vertical line reset voltage VVR via a MOS transistor M8, when it is on, for
15 resetting the vertical signal line V1. Further, the vertical signal line V1 is connected to a capacitor CTN for temporarily storing a noise signal via a noise signal transfer switch M4, and to a capacitor CTS for temporarily storing a photo-charge signal via a photo-charge signal transfer switch M5. The other side of the
20 capacitors CTN and CTS are grounded. A node VIN between the noise signal transfer switch M4 and the capacitor CTN, and a node VIS between the photo-charge signal transfer switch M5 and the capacitor CTS are provided
25 with a voltage VRCT via capacitor reset switches M9 and M10, respectively, when they are on, further, connected

to a differential block 73 for taking the difference between the photo-charge signal and the noise signal via horizontal transfer switches M6 and M7, respectively. The gates of the horizontal transfer switches M6 and M7 are both connected to a column selection line H1, further connected to a horizontal scan circuit 72. For each of the other vertical signal lines V2 to Vn shown in Fig. 13, the identical circuit for reading signals is configured.

Further, the gates of the vertical line reset switches M8, the noise signal transfer switches M4, and the photo-charge signal transfer switches M5, which are provided for each of the vertical signal lines V1 to Vn, are connected to lines VRES, TN, and TS, respectively, to which signals Φ VRES, Φ TN, and Φ TS are provided, respectively.

Next, the operation of the image sensing apparatus as shown in Fig. 13 will be explained below with reference to Fig. 15. Here, a case of reading signals from the pixels in the first row is explained as an example.

In advance of reading of a photo-charge signal from each photodiode PD, the signal Φ RES1, applied to the gates of the reset MOS M1 in the first row, and the signal Φ VRES, applied to the gates of the MOS transistors M8, become high before time t_{71} . Accordingly,

the gates of the MOS amplifier M3 are reset to the voltage VR, and the vertical signal lines V1 to Vn are reset to the voltage VVR. After the signal Φ_{RES1} , applied to the gates of the reset MOS M1, and the signal Φ_{VRES} , applied to the gates of the MOS transistors M8, are changed to low at time t_{71} , the signal Φ_{SEL1} , applied to the gates of the MOS selectors M2 in the first row, and the signal Φ_{TN} applied to the gates of the noise signal transfer switches M4 become high at time t_{72} .

Accordingly, the reset signal VR is superposed with a reset noise, and multiplied by a gain A by the MOS amplifiers M3, further shifted by a gate-source voltage VGS of the MOS amplifiers. Then, the resultant noise signals are read out to the respective capacitors CTN.

The noise signal (voltage) V1N is expressed by the following equation.

$$V_{1N} = A \times (V_R - V_{GS}) \quad \dots (6)$$

Note, the gate-source voltage VGS varies depending upon a threshold voltage Vth of each MOS amplifier M3 in each pixel, as described above.

Thereafter, the signal Φ_{SEL1} , applied to the gates of the MOS selectors M2, and the signal Φ_{TN} applied to the gate of the noise signal transfer switches M4 are changed to low at time t_{73} .

At this time, the voltages of the vertical signal lines V1 to Vn gradually decrease as they are discharged at a time constant determined by parasitic capacitances CP of the vertical signal lines V1 to Vn and the constant current sources (I1). Since the constant current source (I1) is connected to each vertical signal line, even though the voltage VVR for resetting the vertical signal lines V1 to Vn is set to a substantially high voltage and the MOS amplifiers M3 are in the off state at the start of reading signals, the voltages of the vertical signal lines V1 to Vn decrease due to the constant current, and the MOS amplifiers M3 are eventually turned on, thus the signals are read out. Therefore, there is no limitation on the level of reset voltage for the vertical signal lines V1 to Vn.

Next, before transferring the photo-charges, the signal Φ_{VRES} , applied to the gates of the MOS transistors M8, are changed to high at time t_{74} , and the vertical signal lines V1 to Vn are reset to the voltage VVR again. Accordingly, an initial voltage of the vertical signal lines V1 to Vn for reading photo-charge is set to the same voltage as that for reading the noise signals. Therefore, when it is not possible to take a sufficient period since noise signals are read until photo-charges are transferred, an initial potential of the vertical signal line when outputting a noise signal

and an initial potential of the vertical signal line when outputting a photo-charge signal are identical; therefore, noise reduction operation, which will be explained later, is performed at high precision.

5 Thereafter, the signal Φ_{TX1} applied to the gates of the charge transfer switches TX in the first row becomes high at time t_{75} , and the photo-charge generated by the photodiode PD is transferred to the gates of the respective MOS amplifiers M3. After the signal Φ_{TX1}
10 applied to the gates of the charge transfer switches TX is changed to low at time t_{76} and the signal Φ_{VRES} applied to the gates of the MOS transistors M8 is changed to low at time t_{77} , the signals Φ_{SEL1} , applied to the gates of the MOS selectors M2 in the first row, and
15 the signal Φ_{TS} applied to the gates of the photo-charge signal transfer switches M5 become high at time t_{78} . Accordingly, the photo-charge signal (voltage) V_{sig} is amplified by the gain A of the corresponding MOS amplifier M3 and shifted by a gate-source voltage of the
20 MOS amplifier M3, and a resultant voltage is read out to the capacitor CTS. The output voltage V_{1S} is expressed by the following equation (7).

$$V_{1S} = A \times (V_{sig} - V_{GS}) \quad \dots (7)$$

25

Thereafter, the signal ΦSEL1 , applied to the gates of the MOS selectors M2, and the signal ΦTS , applied to the gates of the photo-charge signal transfer switches M5, are changed to low at time t_{79} . At this time, the
 5 voltages of the vertical signal lines V1 to Vn gradually decrease as they are discharged at a time constant determined by parasitic capacitances Cp of the vertical signal lines V1 to Vn and the constant current sources (I1).

10 Then, the signal ΦVRES , applied to the gates of the MOS transistors M8, becomes high at time t_{710} , thereby the signal lines V1 to Vn are reset. With the aforesaid operation, the noise signals and photo-charge signals of the pixels S11 to S1n, connected to the first row, are
 15 stored in the capacitors CTN for storing noise signals and the capacitors CTS for storing photo-charge signals, each provided for the respective columns.

Thereafter, the gates of the horizontal transfer switches M6 and M7 are sequentially changed to high in
 20 response to signals H1 to Hn provided from the horizontal scan circuit 72 at time t_{711} , and the voltages stored in the capacitors CTN and CTS are sequentially outputted to the differential block 73. The differential block 73 takes the differences between the photo-charge
 25 signals V1S to VnS and the corresponding noise signals V1N to VnN, and sequentially outputs the differences as

a voltage VOUT. For example, the output voltage VOUT of the first column is expressed by the following equation, obtained by subtracting equation (6) from equation (7).

5
$$VOUT = V1S - V1N = A \times (Vsig - VR) \dots (8)$$

Therefore, photo-charge signals from which variation in threshold voltages Vth of the MOS amplifiers is reduced for the pixels are outputted.

10 Further, on the right-hand side of equation (8), reset noise is included both in the terms Vsig and VR, therefore, the reset noise is canceled out, and photo-charges generated by the photodiodes PD are amplified and outputted as the output voltages VOUT.

15 With the aforesaid operation, reading of photo-charges from the pixels in the first row is completed. After this, in advance of reading the photo-charges from the second row, a signal Φ_{CTR} , applied to the gates of the reset switches M9 and M10, becomes high, and the
20 gates are reset to the voltage VRCT, and photo-charges of the pixels S21 to S2n connected in the second row are read out. Thereafter, photo-charges of the pixels S31 to Smn connected to the third to m-th row are sequentially read out in response to signals provided from the
25 vertical scan circuit 71 in the similar manner as

described above, and photo-charges are read out from all the pixels.

Regarding the gain A in equation (8), since a source-follower type amplifier has the MOS amplifier M3 whose load is the current source I1, the gain is about 1. Therefore, when the gain of the differential block is set to 1, an unprocessed voltage difference between a photo-charge signal and a noise signal is outputted. Further, since variation in the threshold voltages of the MOS amplifiers M3 and variation in threshold voltages of the reset MOS M1, as well as reset noise are reduced, an image signal of high S/N ratio can be obtained.

Further, in the seventh embodiment as described above, in reading a noise signal and a photo-charge signal to the capacitors CTN and CTS, a capacitive division configuration is not adopted; thus, the capacitances of the capacitors CTN and CTS are not affected by the parasitic capacitance of the vertical output lines, and a small-size solid-state image sensing apparatus as well as high speed reading of the solid-state image sensing apparatus are realized.

<Eighth Embodiment>

Next, the eighth embodiment will be explained.

Fig. 16 is a circuit diagram illustrating a basic configuration of a pixel according to the eighth embodiment of the present invention. Referring to Fig. 16, the basic configuration of each pixel is explained.

5 In Fig. 16, units and elements as those shown in Fig. 14 are referred to by the same references, and a plurality of such pixels are arranged as shown in Fig. 13. Pixels and peripheral circuits are manufactured in CMOS LSI processing, and collectively called as "CMOS sensor".

10 Photodiodes may be formed while forming a source-drain diffusion layer. However, since the photodiodes in the pixels according to the eighth embodiment of the present invention are complete depletion type buried photodiodes, processes for forming the photodiodes are
15 added to standard CMOS LSI processing. With the complete depletion type photodiodes, photo-charges of good linearity can be obtained.

In Fig. 16, the anode of the photodiode PD which generates photo-charge is grounded. The cathode of the
20 photodiode PD is connected to the gate of the MOS amplifier M3 via the charge transfer switch TX. Further, to the gate of the MOS amplifier M3, the source of the reset MOS M1 for resetting the gate of the MOS amplifier M3 is connected, and the drain of the reset MOS M1 is
25 applied with the reset voltage VR. Further, the drain of the MOS amplifier M3 is applied with the operation

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voltage VDD, and the source is connected to the MOS selector M2 for connecting the MOS amplifier M3 to the vertical signal line. Since the MOS selector M2 is connected to the source of the MOS amplifier M3, it is possible to widen the dynamic range in the VDD side, compared against the pixel circuit shown in Fig. 14.

It should be noted that, in the solid-state image sensing apparatus shown in Fig. 13 having the pixels shown in Fig. 16, and the same effects as those of the seventh embodiment are obtained by operating the apparatus in the same manner as that explained in the seventh embodiment.

By operating the solid-state image sensing apparatus according to the eighth embodiment in accordance with operation timing as shown in the timing chart in Fig. 15, noise signals of the respective pixels are read out in a period between time t_{72} and time t_{73} , photo-charge signals are read out in a period between time t_{78} and time t_{79} , and the output signals VOUT, which are the differences between the photo-charge signals and the noise signals, are obtained by the differential block 73.

The output signals VOUT do not include components of threshold voltages V_{th} of the MOS transistors M1 and M3, thus, fixed pattern noise of the CMOS sensor, which has been considered as a problem, is reduced. The both

terms V_{sig} and V_R in the right hand side of equation (8) include reset noise, therefore, the reset noise is canceled out. As a result, a component of the photo-charge generated by the photodiode PD is converted to a voltage, i.e., the output voltage V_{OUT} . Therefore, noise due to variation in the threshold voltage of the amplifier is also reduced, thereby an image signal of high S/N ratio can be obtained.

Further, high-density integration of the CMOS sensor including the vertical scan circuit and the horizontal scan circuit becomes possible, which enables to produce a small-sized image sensor consuming low electrical energy.

Furthermore, since complete depletion type buried photodiodes are used, photo-charges of good linearity can be obtained.

According to the seventh and eighth embodiments as described above, a load for a MOS amplifier is provided and a signal is temporary stored in a capacitor via a source follower, thus, better sensitivity is achieved with a smaller capacitance of the capacitor than a clamping capacitor C_1 (Fig. 17). Accordingly, the chip size of a solid-state image sensing apparatus can be reduced.

A switch for resetting each vertical signal line is provided and, in advance of reading of a photo-charge

signal after reading a noise signal, the vertical signal line is reset to a predetermined reset voltage. Thus, the initial potential of the vertical signal line when outputting a noise signal and the initial potential of the vertical signal line when outputting a photo-charge signal become identical even when reading these signals at high speed. Accordingly, noise can be easily reduced at high precision.

Further, by providing a load for the MOS amplifier, even when the reset voltage for resetting the vertical signal line is set relatively high and the MOS amplifier is in the off state in an early stage of reading a photo-charge signal, the voltage of the vertical signal line decreases in response to the constant current of the load, and the MOS amplifier is eventually turned on. Accordingly, the photo-charge signal is read out. Therefore, there is no limitation on the reset voltage to be applied to the vertical signal line.

Furthermore, each vertical signal line is reset before reading noise as well as before reading photo-charge, thus the vertical signal line is refreshed each time signals is read from a pixel. Accordingly, it is possible to restrict interference between adjoining pixels as well as prevent cross modulation and blooming.

Note that, in the above embodiments, NMOS transistors are mainly used in the circuits, however,

the present invention is not limited to this, and it is possible to use PMOS transistors in place of the NMOS transistors. Further, the field effect transistors are not limited to the MOS type.

5 As many apparently widely different embodiments of the present invention can be made without departing from the spirit and scope thereof, it is to be understood that the invention is not limited to the specific embodiments thereof except as defined in the appended
10 claims.